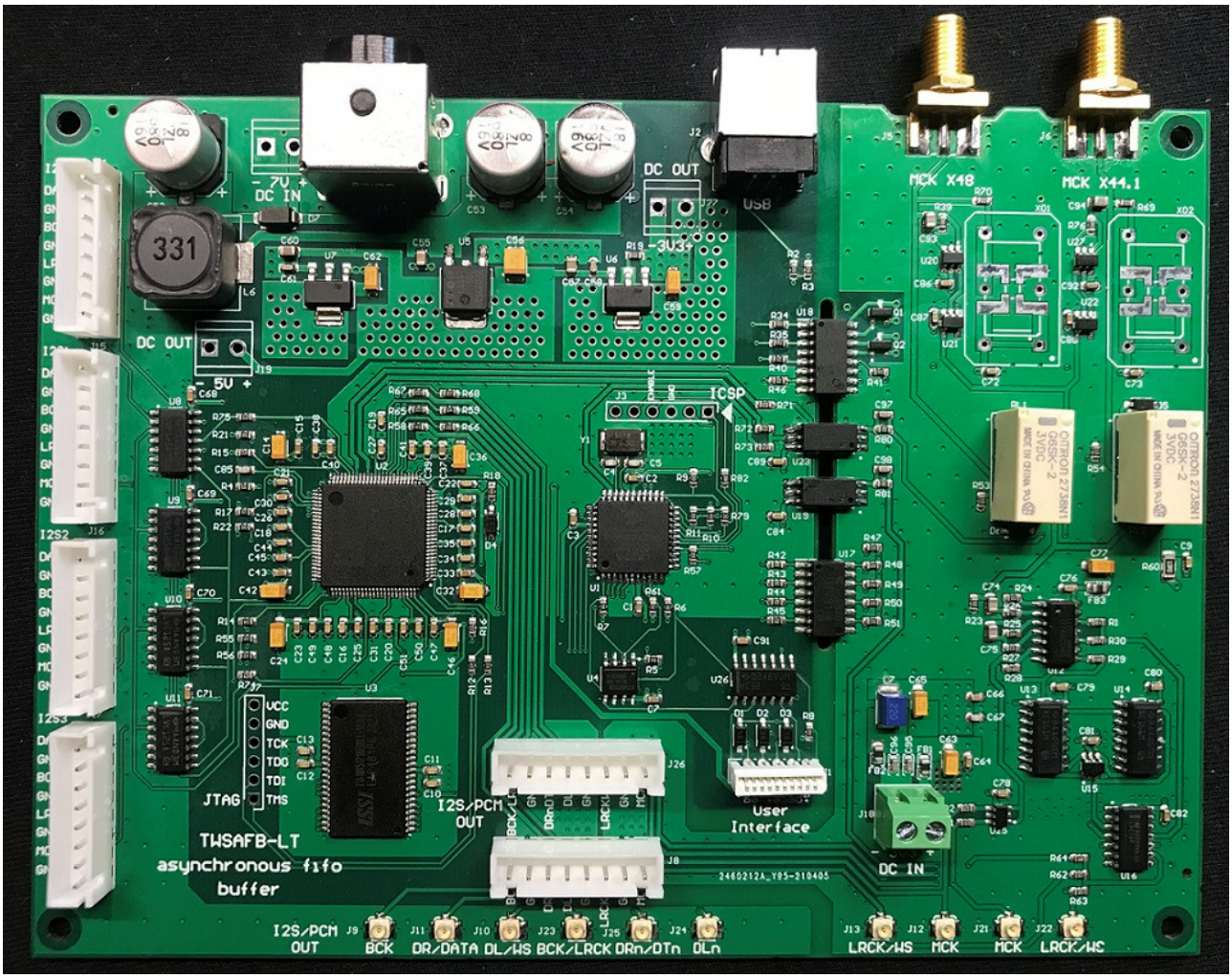
TWSAFB-LT The Well Synchronized Asynchronous FIFO buffer



The TWSAFB-LT is an asynchronous FIFO buffer intended to isolate the DAC from the source, getting them operating in different and fully isolated time domains. This way the jitter of the source cannot affect the DAC. Practically the incoming I2S data are stored in a buffer memory. Then they are processed by an FPGA which works in slave mode. This means that the outgoing data are synchronized in a different time domain managed by the master clock and optically isolated from the incoming data, preventing source jitter from crossing the FIFO and affecting the DAC. In practice, this allows the output signals to be regenerated starting from a much more precise clock than that of the source.

The TWSAFB-LT FIFO buffer provides digital outputs to drive most of the DAC on the market, both modern sigma-delta DACs like SABRE and AKM and even old multi-bit DAC like TDA1541A, PCM1704 and so on. It provides I2S, PCM and DSD output.

In DSD output format the Return to Zero logic is available to get the best performance from DSD DAC. RTZ logic allows to null rise/fall time errors which occur in the DAC switches.

The FIFO Lite accepts I2S, DoP and DSD inputs up to 32 bit/384 kHz and up to DSD512. It provides 4 selectable inputs on JST 8-pin headers.

The outputs are available on 8-pin JST headers or separately on u.fl connectors. Both PCM and I2S output are available in stopped clock and continuous clock modes (this second option is applied only when the output bit depth is divisible from the master clock frequency). DSD output is only available in continuous clock since the SCK is taken directly from the master clock in order to minimize the jitter effect. It can drive balanced and unbalanced DAC in DSD output format.

The part of the circuit containing the master clock, the conversion from sine wave to square wave and the dividers is powered separately and isolated from the rest of the circuit which handles the input signals.

The TWSAFB-LT needs one or two master clock (one for each sample rate family) in order to work. Two on-board SMA connectors are provided for master clock inputs. The FIFO Lite accepts both sine (up to +18dBm) and square wave (CMOS 3V3 to 5V) oscillators as the master clock. Although there are footprints to install Crystek, Accusilicon and NDK oscillators, it's strongly recommended to provide better clocks like the TWTMC-DRIXO. The best phase noise performance is reached with 5.6448 MHz and 6.144 MHz DRIXO oscillators (when these master clock frequencies are sufficient for DAC you are planning to drive).

The clock selection is managed by double coil latching relay in T configuration to get better isolation between the two clocks and to avoid the master clock crossing active devices which inevitably add jitter.

The sine to square converter used in the FIFO Lite is virtually jitter free. This means that after the conversion the resulting square wave has almost the same phase noise of the sine wave oscillators. The configuration of the dividers used in the FIFO Lite allows to further improve the phase noise at the LRCK output. This allows to get the best performance as possible from the DACs which switch by the LRCK or MCK signal.

The TWSAFB-LT implements 8 selectable dither depth separately for each source (to be used in case of data truncation, for example 24 to 16 bit for the TDA1541A). Dithering is not available in DSD output mode.

The TWSAFB-LT implements 8 selectable buffer depth separately for each source, from 65kb to 8Mb. This defines the latency of the FIFO from the minimum (65kb) up to the maximum (8Mb).

All the FIFO Lite settings can be configured one time by connecting it to a PC using the on-board USB connector. The Windows application which manages the settings can be downloaded from the website.

The FIFO Lite can apply a digital DAC calibration to reach the best DAC accuracy. Calibration data file can be uploaded by the Windows application. DAC calibration is not available in DSD output mode.

An optional user interface board can be used to manage some function on the fly like source selection, dither, enable/disable DAC calibration and so on. The user interface also shows the

sample rate, the selected source and the selected dither. It also provides any error messages encountered during configuration and normal operation.

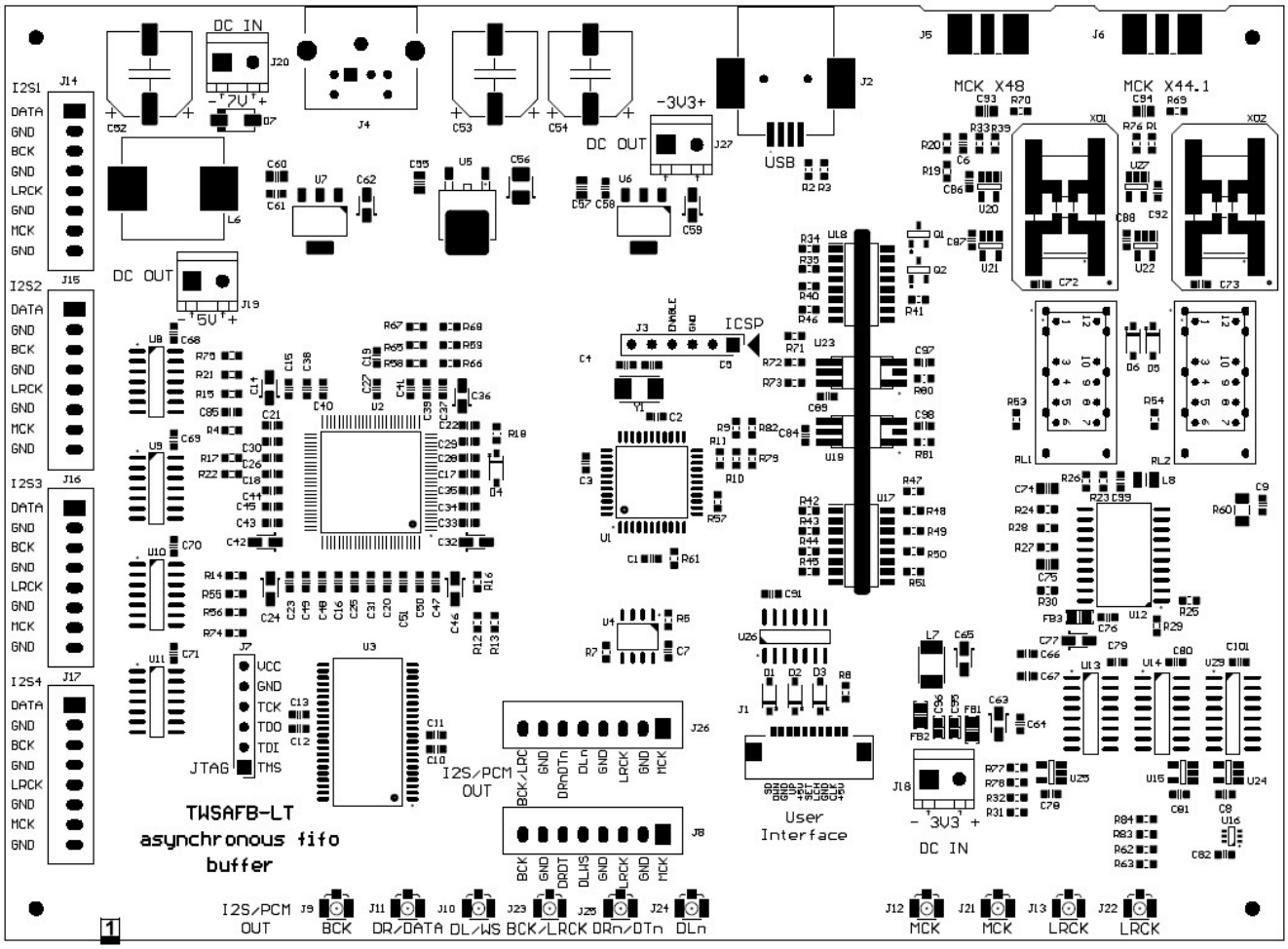
The micro controller used in the FIFO Lite to manage its functions turns in standby mode during listening. This way there isn't any RF interference at all which can affects the digital output signals.

Features:

Input format: I2S/DoP/DSD
Inputs: 4 x selectable inputs
Output format: compatible with almost all modern and old DACs (I2S/PCM/DSD)
Custom output format: for TDA1541A (offset binary), TWSDAC-LT DAC Lite, Soekris DAM1021 upgrade, AD5791, TDA1541A and AD1862 dual mono sign magnitude
Clock mode: stopped or continuous clock
Dither: 8 x selectable dither depth separately for each source, not available in DSD mode (used in case of data truncation, for example 24 to 16 bit for the TDA1541A)
FIFO buffer depth: 8 x selectable buffer depth separately for each source, from 65kb to 8Mb
Optional: digital DAC calibration to reach the best precision, TWSDAC-LT DAC Lite and maybe other DACs (not available in DSD mode); Return to Zero logic for DSD output format
Configuration: all settings can be configured one time by USB connection to the Windows application
Optional: user interface to manage some function on the fly like source selection, dither, enable/disable DAC calibration and so on
Master Clock selection: T-switch configuration relay to select the sample rate family instead of multiplexers
Optical isolation: MCK and LRCK optical isolated from the FPGA and the micro to avoid interferences (BCK with the TWSAFB-OIR re-clocker board)
External Master Clock: SMA connectors for external clocks
No RF: micro controller in standby during listening (no RF interference at all)
Direct clock output: LRCK/MCK directly from the Master clock (optical isolation) instead of from the FPGA
Phase noise: very low phase noise outputs (MCK, LRCK, BCK with TWSAFB-OIR board)
Board size: 160 x 117 mm

Note: finished board (without oscillators).

PCB layout



Connectors

J14-J15-J16-J17: I2S1-I2S2-I2S3-I2S4, I2S inputs

1. DATA, I2S DATA, DoP DATA, DSD DATA Left
2. GND, Ground
3. BCK, I2S bit clock, DSD SCK
4. GND, Ground
5. LRCK, I2S word select, DSD DATA Right
6. GND, Ground
7. MCK, master clock
8. GND, Ground

J5: MCK x48, external master clock for x48 sample rate family (6.144 MHz to 24.576 MHz)

J6: MCK x44.1, external master clock for x44.1 sample rate family (5.6448 MHz to 22.5792 MHz)

J20: Main power supply (FPGA, micro), 7 VDC/200 mA

J4: Main power supply alt. (FPGA, micro), 7 VDC/200 mA, 6-pin DIN, suitable male plug CUI Devices MD-60 (Mouser part 490-MD-60)

1. Ground
2. Ground
3. Ground
4. Ground
5. +7 VDC
6. +7 VDC

J18: Auxiliary power supply (master clock, squarer, dividers), 3.3 to 5 VDC/30 mA

J27: USB, USB type B input to connect the board to PC

J1: User interface output to connect to TWSAFB-UI, suitable FPC cable Molex 15267-0260 (Mouser part 538-15267-0260)

J19: DC OUT, 5 VDC/50 mA power supply output (can be used to power the TWSAFB-RX)

J27: DC OUT, 3.3 VDC/50 mA power supply output (don't connect to J18)

J7: Reserved, leave unconnected

J3: FIFO initialized and running

1. Reserved, leave unconnected
2. Reserved, leave unconnected
3. Enable (high level as soon as the FIFO has been initialized)
4. Ground
5. Reserved, leave unconnected
6. Reserved, leave unconnected

XO1: on-board MCK x48 oscillator, sine wave up to +18dBm or CMOS up to 5V, 6.144 MHz to 24.576 MHz

XO2: on-board MCK x44.1 oscillator, sine wave up to +18dBm or CMOS up to 5V, 5.6448 MHz to 22.5792 MHz

J12-J21: Master clock outputs or DSD SCK, CMOS 3.3 to 5V depending on the voltage applied to J18

J13-J22: LRCK outputs, CMOS 3.3 to 5V depending on the voltage applied to J18, stopped clock mode only

J9: BCK, I2S/PCM bit clock output

J11: DR/DATA, PCM Right DATA output (stopped clock), I2S DATA output (continuous clock), DSD Right DATA output

J10: DL/WS, PCM Left DATA output (stopped clock), I2S WS output (continuous clock), DSD Left DATA output

J23: BCK/LRCK, PCM Bit clock output (dual stopped clock), PCM LRCK output (continuous clock)

J25: DRn/DTn, PCM complementary Right DATA output (dual stopped clock), I2S complementary DATA output (stopped clock), DSD complementary Right DATA output

J24: DLn, PCM complementary Left DATA output (dual stopped clock), DSD complementary Left DATA output

J8: I2S/PCM output

1. BCK, Bit clock
2. GND, Ground
3. DRDT, Right Data (PCM stopped clock), Data (I2S stopped clock), DSD Right Data
4. DLWS, Left Data (PCM stopped clock), WS (I2S continuous clock), DSD Left Data
5. GND, Ground
6. LRCK, LRCK (PCM stopped clock), WS (I2S stopped clock)
7. GND, Ground
8. MCK, Master clock or DSD SCK

J26: I2S/PCM output

1. BCK/LRC, Bit clock (PCM stopped clock), LRCK (PCM continuous clock)
2. GND, Ground
3. DRnDTn, PCM complementary Right DATA output (dual stopped clock), I2S complementary DATA output (stopped clock), DSD complementary Right DATA
4. DLn, PCM complementary Left DATA output (dual stopped clock), DSD complementary Left DATA
5. GND, Ground
6. LRCK, LRCK (PCM stopped clock), WS (I2S stopped clock)
7. GND, Ground
8. MCK, Master clock or DSD SCK

There is 1 available option for this board: finished board without master clocks

Master clocks connection

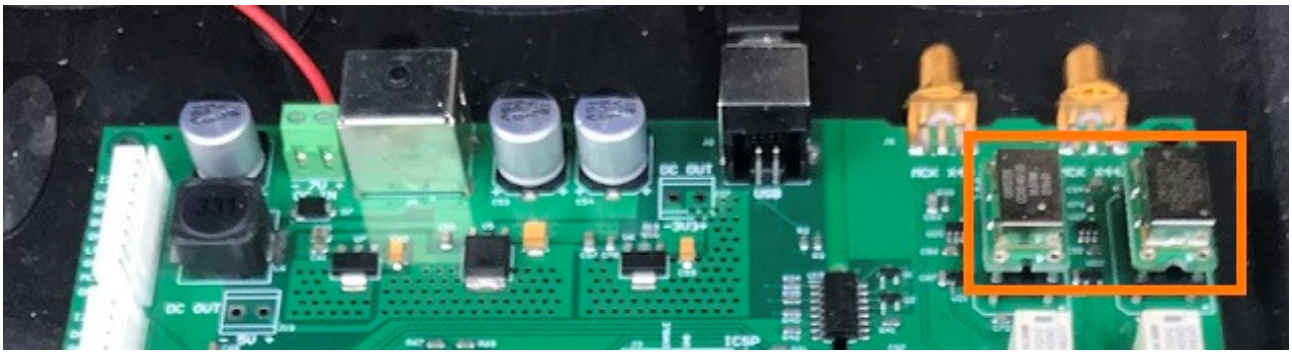
In order to get the FIFO Lite working one or two master clocks have to be provided.

There are two ways to connect the master clocks to the TWSAFB-LT: J5 and J6 SMA connectors for external oscillators or XO1 and XO2 footprints for on-board oscillators. J5 and XO1 are reserved for the oscillator which manages the x48 sample rate family, while J6 and XO2 are reserved for the oscillator which manages the x44.1 sample rate family. Allowed master clock frequencies are 5.6448 MHz up to 22.5792 MHz for the x44.1 sample rate family and 6.144 MHz up to 24.576 MHz for the x48 sample rate family.

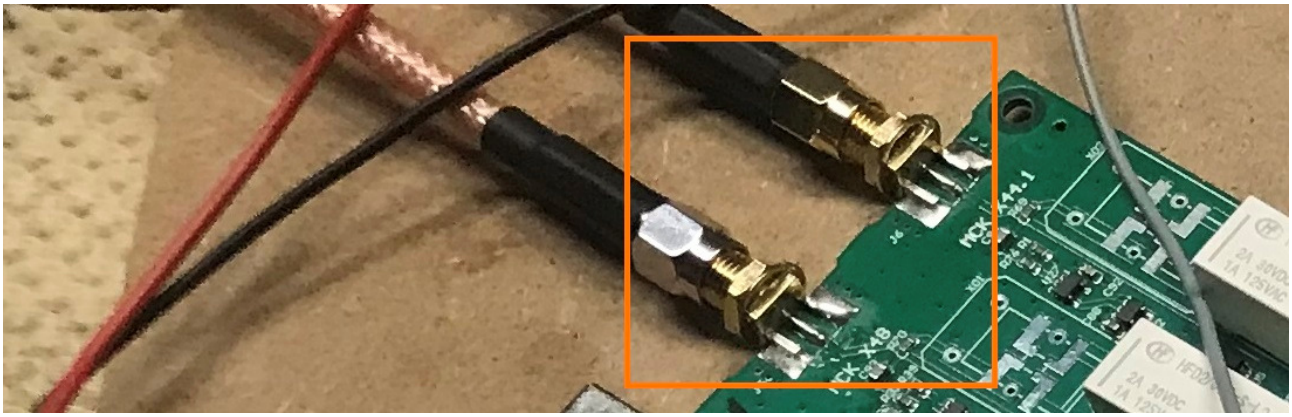
In case the oscillators was reversed the FIFO Lite will not work. The FIFO Lite will work with a single oscillator, but of course only one sample rate family will be allowed.

The FIFO Lite accepts both sine wave (up to +18dBm) and square wave (CMOS up to 5V) oscillators on both SMA and footprints inputs. Footprints accommodate several commercial oscillators like Crystek, Accusilicon and NDK. These can be installed directly on the footprints or by DIL sockets.

It's recommended to install the best oscillators as possible to get the best phase noise performance from the FIFO Lite. The best options are the TWTMC-DRIXO oscillators which are state of the art devices. Lowest phase noise is achieved using the lowest frequencies as possible (5.6448 MHz and 6.144 MHz).



Crystek oscillators installed on-board.



External oscillators connected to the SMA connectors.

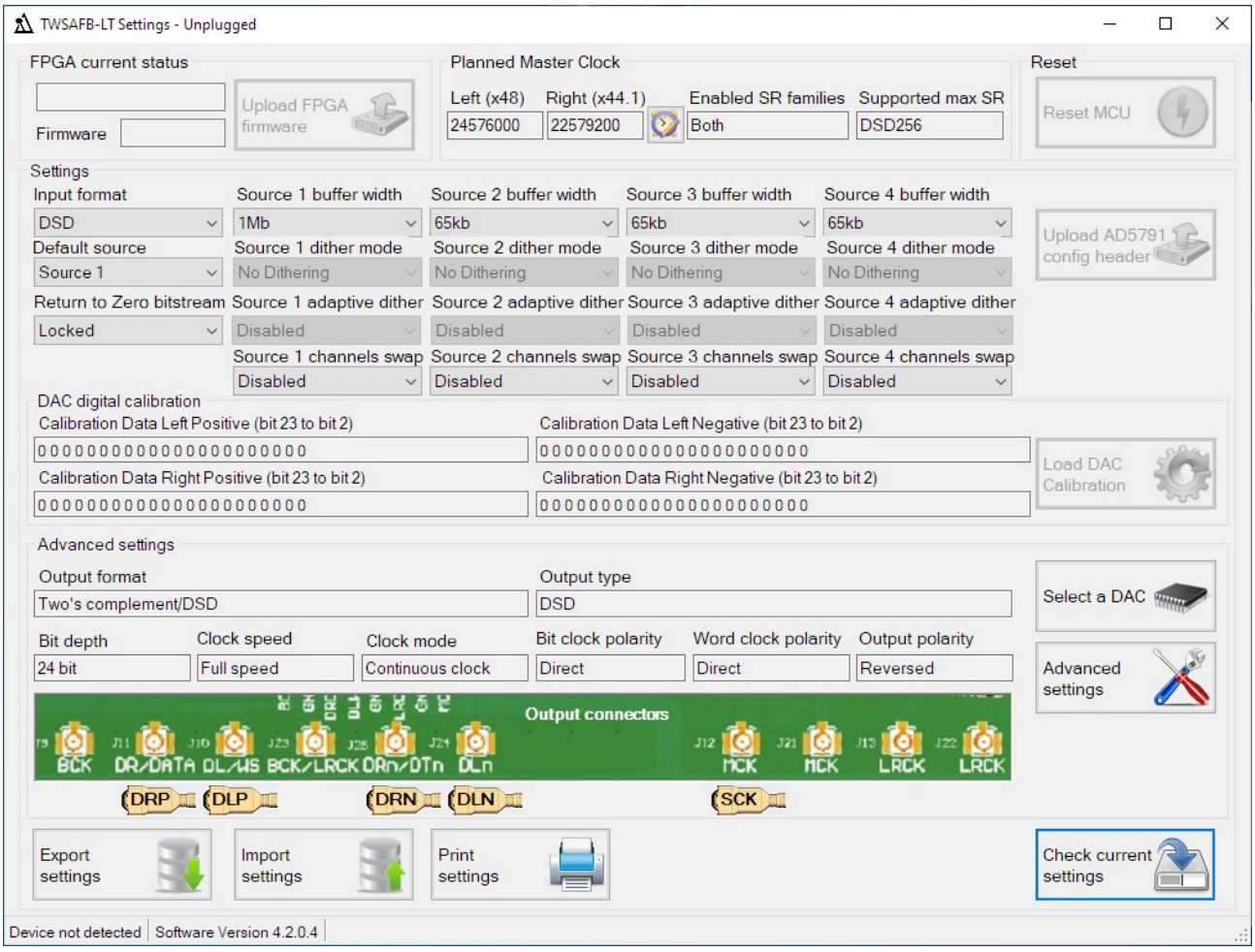
Powering and configuring the TWSAFB-LT (FIFO Lite)

In order to get the FIFO Lite properly working with the DAC you are planning to drive some settings have to be configured. Settings can be configured one time and stored in the EEPROM of the microcontroller. It will be necessary to update the settings only if the DAC to be driven is replaced.

The configuration is managed by the Windows application TWSAFB-LT Settings. The application can be used even in unplugged mode (without the FIFO Lite connected) to check DAC compatibility and settings. The application can be downloaded from the FIFO Lite website page at the following link and will be automatically updated when a new version is available at startup:

https://www.thewellaudio.com/wp-content/uploads/App/TWSAFBLTSet/TWSAFBLTSet.application

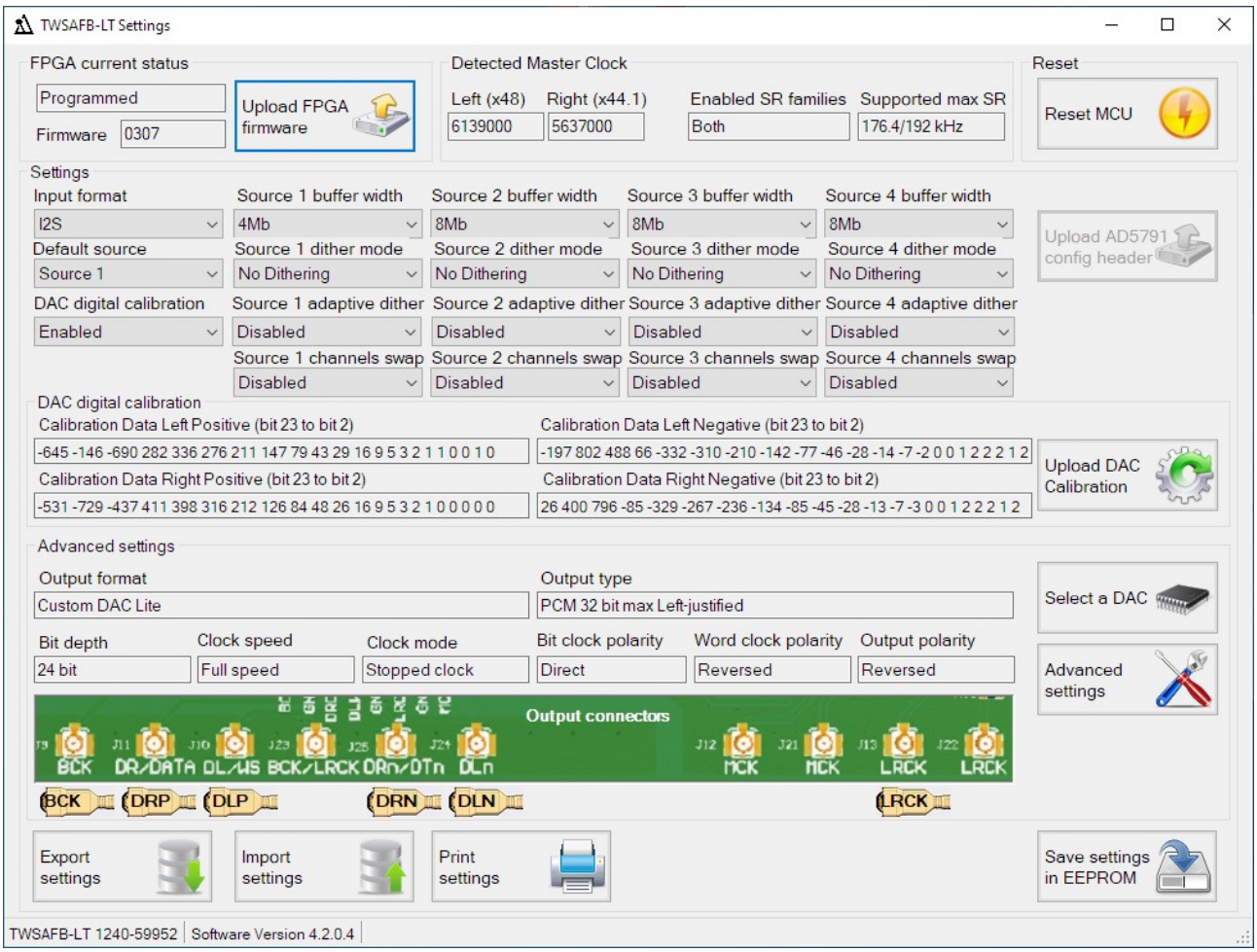
Prerequisites:
64-bit operating system like Microsoft Windows 7 or later
Microsoft .NET Framework 4 or later
Windows Installer 3.1 or later



Windows application working in unplugged mode

Startup sequence:

1. Download and install the Windows application TWSAFB-LT Settings
2. Connect one or two master clock oscillators to the FIFO Lite
3. Power on the oscillators
4. Provide main power supply to the FIFO Lite J20 connector (7 VDC/200 mA)
5. Provide auxiliary power supply to the FIFO Lite J18 connector (3.3 to 5 VDC/30 mA)
6. Connect the USB cable to the FIFO Lite J27 connector
7. Connect the FPC cable from the FIFO Lite to the TWSAFB-UI user interface (if you have one)
8. Power on the FIFO Lite
9. Run the Windows application
10. Wait until the oscillators and the device are detected



Once the oscillators and the device have been detected the application shows:

- Detected device (TWSAFB-LT 1240-59952)
- Detected Master Clock frequencies (12333000 and 11332000 in the above picture)
- FPGA Firmware version (0307 in the above picture)
- Software Version (4.2.0.4 in the above picture)
- Current settings (Custom DAC Lite with Digital Calibration Enabled, default settings if never configured)

Let examine the functionality and the parameters to be set from the top-left to the bottom-right.

FPGA current status group

This group of controls manage the FPGA firmware.

If the firmware has never been uploaded the current status is "Not programmed", otherwise the current firmware version is displayed. If you are connected to the internet the application automatically check for a newer firmware version as startup. If a newer version is available the application asks the user to upload it. Pressing Ok button the new firmware version will be uploaded. If the new FPGA firmware is loaded correctly the application issues the information message "Firmware uploaded successfully". If the uploading fails the application brings an error message like "Failed uploading Firmware," followed by the specific reason which causing the error.

FPGA firmware can also be loaded offline, you can download the last version at the following link: https://www.thewellaudio.com/wp-content/uploads/TWSAFB-LT_FPGA_firmware.zip

Once the firmware has been download press the "Upload FPGA firmware" button and select the .bin file from the folder where it was saved.

Once the firmware has been loaded successfully, the MCU is automatically reset in order to load the firmware in the FPGA. It will take a few seconds to get the FIFO Lite restarted.

Detected Master Clock group

This group of controls manages the master clocks connected to the FIFO Lite.

In unplugged mode it is not possible to detect the master clock, so the button in the center of the group is enabled in order to allow the user to select the master clock frequencies he plans to use. This allows to know the max allowed sample rate as function of the master clock frequencies and the planned DAC to be driven.

In plugged mode the application waits until the MCU of the FIFO Lite detects the installed master clocks. This could take more than 1 minute if one master clock is missing because the MCU tries several times to measure both frequencies before stopping the detection. At the end of the master clock measurement, the application displays the detected frequencies in the text boxes labeled "Left (x48)" and "Right (x44.1)". If a master clock is missing, its text box displays the value 0.

As function of the installed master clock the application displays the "Enabled SR families":

- Both, if both master clock oscillators have been detected
- x48, if only the x48 sample rate family oscillator was detected
- x44.1, if only the x44.1 sample rate family oscillator was detected

Finally the application computes and displays the maximum sample rate supported as function of the installed master clock and the other settings related to the DAC to be driven:

- 352.8/384 kHz, both master clock oscillators detected (DSD512 or DSD256 with RTZ Locked)
- 384 kHz, only the x48 master clock oscillator detected (DSD512 or DSD256 with RTZ Locked)
- 352.8 kHz, only the x44.1 master clock oscillator detected (DSD512 or DSD256 with RTZ Locked)

- 176.4/192 kHz, both master clock oscillators detected (DSD256 or DSD128 with RTZ Locked)
- 192 kHz, only the x48 master clock oscillator detected (DSD256 or DSD128 with RTZ Locked)
- 176.4 kHz, only the x44.1 master clock oscillator detected (DSD256 or DSD128 with RTZ Locked)
- 88.2/96 kHz, both master clock oscillators detected (DSD128 or DSD64 with RTZ Locked)
- 96 kHz, only the x48 master clock oscillator detected (DSD128 or DSD64 with RTZ Locked)
- 88.2 kHz, only the x44.1 master clock oscillator detected (DSD128 or DSD64 with RTZ Locked)
- 44.1/48 kHz, both master clock oscillators detected (DSD64 with RTZ disabled)
- 48 kHz, only the x48 master clock oscillator detected (DSD64 with RTZ disabled)
- 44.1 kHz, only the x44.1 master clock oscillator detected (DSD64 with RTZ disabled)

If the installed master clocks and the specific DAC settings don't allow to compute a valid maximum supported sample rate (less than 44.1 kHz or less than DSD64) the application displays the value "Invalid" and the current settings are not accepted.

Reset group

This group contains the button which performs the MCU reset. Pressing this button the MCU of the FIFO Lite will be restarted. It will take a few seconds to get the FIFO Lite restarted.

Settings group - general settings

This group of controls allows to configure all the FIFO Lite general settings.

The Input format dropdown list allows the user to select the data format expected as input. The FIFO Lite provides 3 input formats:

1. I2S, standard I2S format
2. DoP, DSD over PCM format
3. DSD, native DSD format

The "Default source" dropdown list allows the user to select the default source which will be set at FIFO Lite startup. The FIFO Lite provides 4 I2S inputs, so you can select "Source 1", "Source 2", "Source 3" or "Source 4".

For each available source from 1 to 4 you can set 4 individual parameters by the related dropdown list. These parameters are:

1. Buffer width, which defines the depth of the FIFO and the resulting latency
    - 65kb, lowest latency, 23ms at 44.1kHz to 2.6ms at 384kHz
    - 130kb, 46ms at 44.1kHz to 5.2ms at 384kHz
    - 260kb, 92ms at 44.1kHz to 10.4ms at 384kHz
    - 520kb, 184ms at 44.1kHz to 21ms at 384kHz
    - 1Mb, 354ms at 44.1kHz to 41ms at 384kHz
    - 2Mb, 708ms at 44.1kHz to 82ms at 384kHz

    - 4Mb, 1417ms at 44.1kHz to 164ms at 384kHz
    - 8Mb, highest latency, 2834ms at 44.1kHz to 325ms at 384kHz
2. Dither mode, which defines the type of dithering to be applied (not available with DSD input format)
    - No dithering, dither will not be applied
    - HF shaped level 1
    - HF shaped level 2
    - HF shaped level 3
    - HF shaped level 3
    - HF shaped level 4
    - HF shaped level 6
    - 2-LSB Triangular
3. Adaptive dither which defines if selected dithering mode is applied anyway (not available with DSD input format)
    - Disable, the selected dither mode is always applied
    - Enable, the selected dither mode is only applied if data truncation occurs
4. Channels swap which defines if left and right channels are swapped or not
    - Disable, channels are not swapped
    - Enable, channels are swapped (left to right and right to left)

The "DAC digital calibration" dropdown list is only available if a calibration data file has been uploaded (not available with DSD input format). Select "Enabled" if you want the FIFO Lite to apply calibration data. Otherwise, select "Disabled".

The Return to Zero bitstream dropdown list, available with DSD format, allows to enable/disable/lock the RTZ logic in order to null the rise/fall time errors.
Select "Enabled" if you want the FIFO Lite to apply RTZ logic when possible (when the sample rate is equal or lower than the half of the master clock frequency); for higher sample rate RTZ is not applied.
Select "Locked" if you want the FIFO Lite to apply always RTZ logic (when the sample rate is equal or lower than the half of the master clock frequency); higher sample rate is not supported.
Otherwise, select "Disabled", FIFO Lite does not apply RTZ logic.
In every case, RTZ will be applied when the sample rate is equal or lower than the half of the master clock frequency (for example up to DSD256 with 22.5792 and 24.576 MHz master clock, up to DSD128 with 11.2896 and 12.288 MHz master clock and so on).

<u>Settings group - DAC digital calibration (not available with DSD input format)</u>

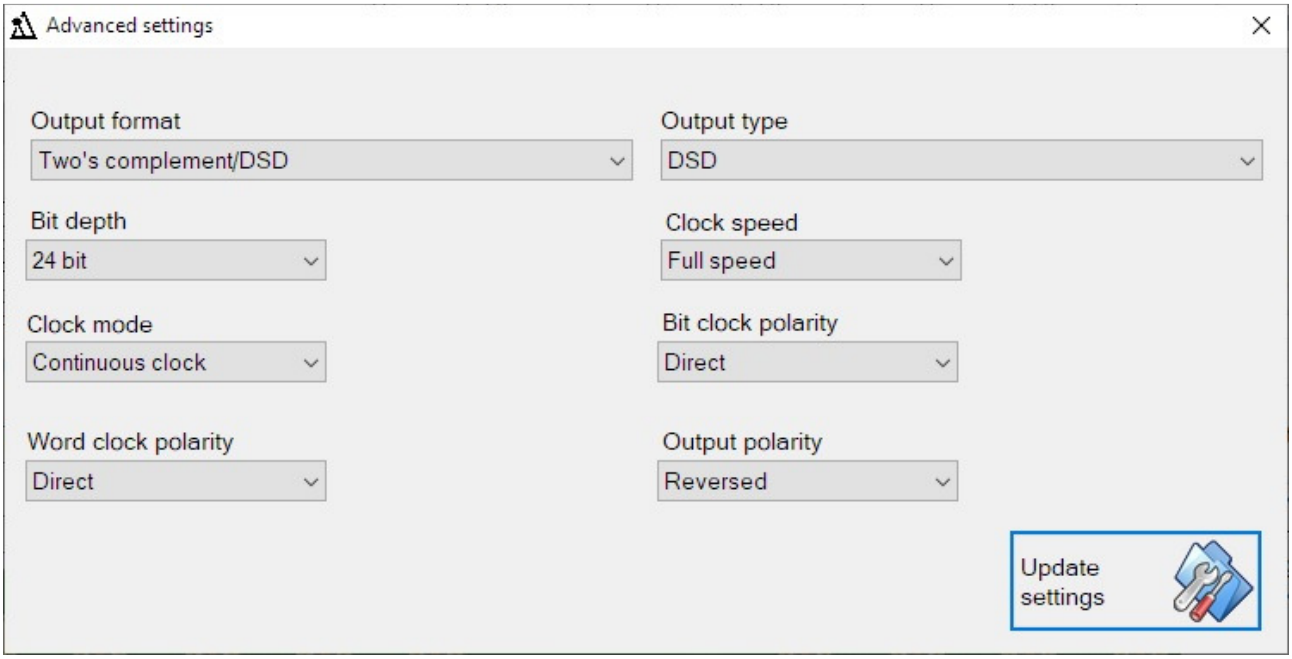
Press "Load DAC calibration" to upload a calibration data file if you have one. This allows to upload and store a file which contains calibration data to be used by the FIFO Lite processor in order to improve the accuracy of the DAC.

Select the .cal file from the folder where it was saved and press "Open". If the calibration data are loaded correctly the application issues the information message " DAC calibration data uploaded successfully". If the uploading fails the application brings the error message like "Failed uploading DAC calibration data, please try again".

Settings group - Advanced settings

This group of text boxes display the DAC specific settings. Press "Advanced settings" to access for update the DAC specific parameters. Be careful to update these settings as the DAC may no longer work properly. In fact the application brings the warning message "Be careful updating advanced settings, use the Select a DAC button instead. Continue?".

If you press Yes a new form is shown which allows to change the DAC specific settings:



1. Output format, which defines the specific output format according to the planned DAC
    - Two's complement/DSD, most DACs need this format
    - Offset binary (TDA1541A), TDA1541A specific output format
    - Custom DAC Lite, TWSDAC-LT DAC Lite specific output format
    - Custom DAM1021 upgrade, Soekris DAM1021 upgrade specific output format
    - Custom Dual complementary PCM, specific output format for DACs which can accept sign magnitude notation (TWSDAC-1862). Two DACs are required for each channel, one for the positive part and the other for the negative part of the signal. MSB never switching at zero crossing.
    - Custom Dual complementary Offset binary, specific output format for TDA1541A running in sign magnitude notation (TWSDAC-1541). Two DACs (1 chip) are required for each channel, one for the positive part and the other for the negative part of the signal. MSB never switching at zero crossing.
    - Custom AD5791, specific output format for AD5791 running in sign magnitude notation (TWSDAC-AD5791). Two DACs are required for each channel, one for the positive part and the other for the negative part of the signal. MSB never switching at zero crossing.

2. Output type, which defines the specific output type according to the planned DAC
    - PCM 16 bit, fixed 16 bit PCM, allowed only with continuous clock

- PCM 32 bit max Left-justified, variable bit depth PCM, allowed only with stopped clock
- PCM 32 bit max Right-justified, right-justified variable bit depth PCM, allowed only with continuous clock
- DSD, DSD allowed only with DoP/DSD Input format
- I2S 16 bit, fixed 16 bit I2S, allowed only with continuous clock
- I2S 32 bit max, variable bit depth I2S, allowed only with continuous clock
- Alternating LR (I2S type) 32 bit max Right-justified, right-justified variable bit depth I2S, allowed only with continuous clock

3. Bit depth, which defines the number of output bits
    - 16 bit, 16 bit data
    - 18 bit, 18 bit data
    - 20 bit, 20 bit data
    - 24 bit, 24 bit data

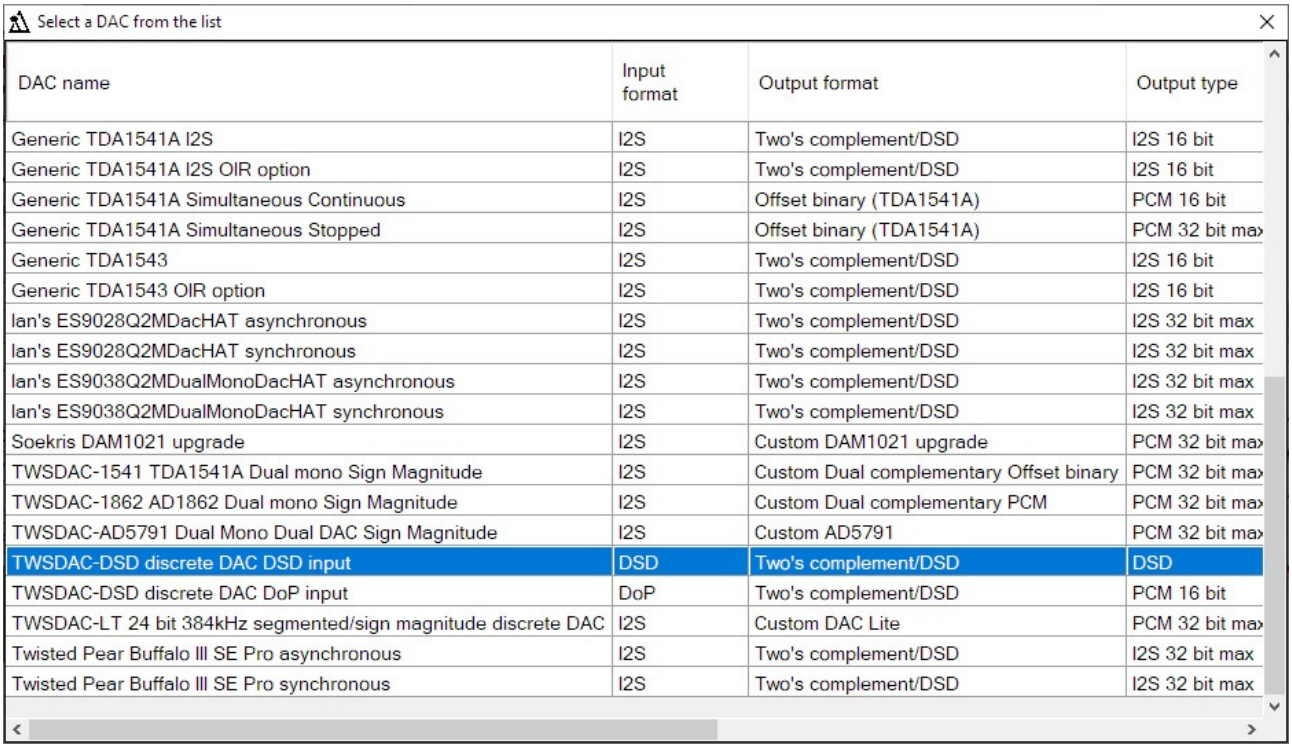
4. Clock speed, which defines the speed of the outgoing data
    - Full speed, the output data is transferred at the maximum possible speed according to master clock, output format and output type
    - Half speed, the output data is transferred at half the maximum possible speed according to master clock, output format and output type (mandatory if the TWSAFB-OIR is installed or in case the planned DAC works asynchronous)
    - Quarter speed, the output data is transferred at a quarter of the maximum possible speed according to master clock, output format and output type (mandatory if the TWSAFB-OIR is installed and the planned DAC works asynchronous)
5. Clock mode, which defines if the bit clock is continuous or is stopped as soon as all data has been transferred
    - Stopped clock, bit clock stops as soon as all data has been transferred, allowed only with PCM 32 bit max Left-justified output type
    - Continuous clock, bit clock never stops, data flow is continuous

6. Bit clock polarity, which defines whether the bit clock is direct or inverted with respect to the other signals
    - Direct, no bit clock inversion
    - Reversed, bit clock is inverted with respect to the other signals

7. Word clock polarity, which defines whether the word clock is direct or inverted with respect to the other signals
    - Direct, no word clock inversion
    - Reversed, word clock is inverted with respect to the other signals

8. Output polarity, which defines whether the output is direct or inverted with respect to the other signals, required for sign magnitude architecture DACs
    - Direct, no output inversion
    - Reversed, output is inverted

Instead of manually configuring the DAC specific settings is recommended to press the button "Select a DAC", to pick one from the DACs database. The DACs in the database are already configured with their specific settings. In this way the configuration is simpler and faster, and above all it avoids running into configuration errors that could cause the planned DAC to malfunction.



DAC name	Input format	Output format	Output type
Generic TDA1541A I2S	I2S	Two's complement/DSD	I2S 16 bit
Generic TDA1541A I2S OIR option	I2S	Two's complement/DSD	I2S 16 bit
Generic TDA1541A Simultaneous Continuous	I2S	Offset binary (TDA1541A)	PCM 16 bit
Generic TDA1541A Simultaneous Stopped	I2S	Offset binary (TDA1541A)	PCM 32 bit max
Generic TDA1543	I2S	Two's complement/DSD	I2S 16 bit
Generic TDA1543 OIR option	I2S	Two's complement/DSD	I2S 16 bit
Ian's ES9028Q2MDacHAT asynchronous	I2S	Two's complement/DSD	I2S 32 bit max
Ian's ES9028Q2MDacHAT synchronous	I2S	Two's complement/DSD	I2S 32 bit max
Ian's ES9038Q2MDualMonoDacHAT asynchronous	I2S	Two's complement/DSD	I2S 32 bit max
Ian's ES9038Q2MDualMonoDacHAT synchronous	I2S	Two's complement/DSD	I2S 32 bit max
Soekris DAM1021 upgrade	I2S	Custom DAM1021 upgrade	PCM 32 bit max
TWSDAC-1541 TDA1541A Dual mono Sign Magnitude	I2S	Custom Dual complementary Offset binary	PCM 32 bit max
TWSDAC-1862 AD1862 Dual mono Sign Magnitude	I2S	Custom Dual complementary PCM	PCM 32 bit max
TWSDAC-AD5791 Dual Mono Dual DAC Sign Magnitude	I2S	Custom AD5791	PCM 32 bit max
TWSDAC-DSD discrete DAC DSD input	DSD	Two's complement/DSD	DSD
TWSDAC-DSD discrete DAC DoP input	DoP	Two's complement/DSD	PCM 16 bit
TWSDAC-LT 24 bit 384kHz segmented/sign magnitude discrete DAC	I2S	Custom DAC Lite	PCM 32 bit max
Twisted Pear Buffalo III SE Pro asynchronous	I2S	Two's complement/DSD	I2S 32 bit max
Twisted Pear Buffalo III SE Pro synchronous	I2S	Two's complement/DSD	I2S 32 bit max

Double click on the row which represents the planned DAC and all the specific settings will be applied. More DAC. Other DACs can be added to the database if not listed.

Once the DAC settings have been chosen the application displays how the output connectors have to be connected with the DAC.

For example in the above image the connections to the TWSDAC-DSD DAC are shown. For each u.fl socket, the relevant connector is displayed only if it must be used. On each u.fl connector to be used, the application applies a label indicating which DAC input it must be connected to.

Final operations

In unplugged mode the button at the bottom-right of the form is labeled "Check current settings" and is used to check if the selected settings are correct.

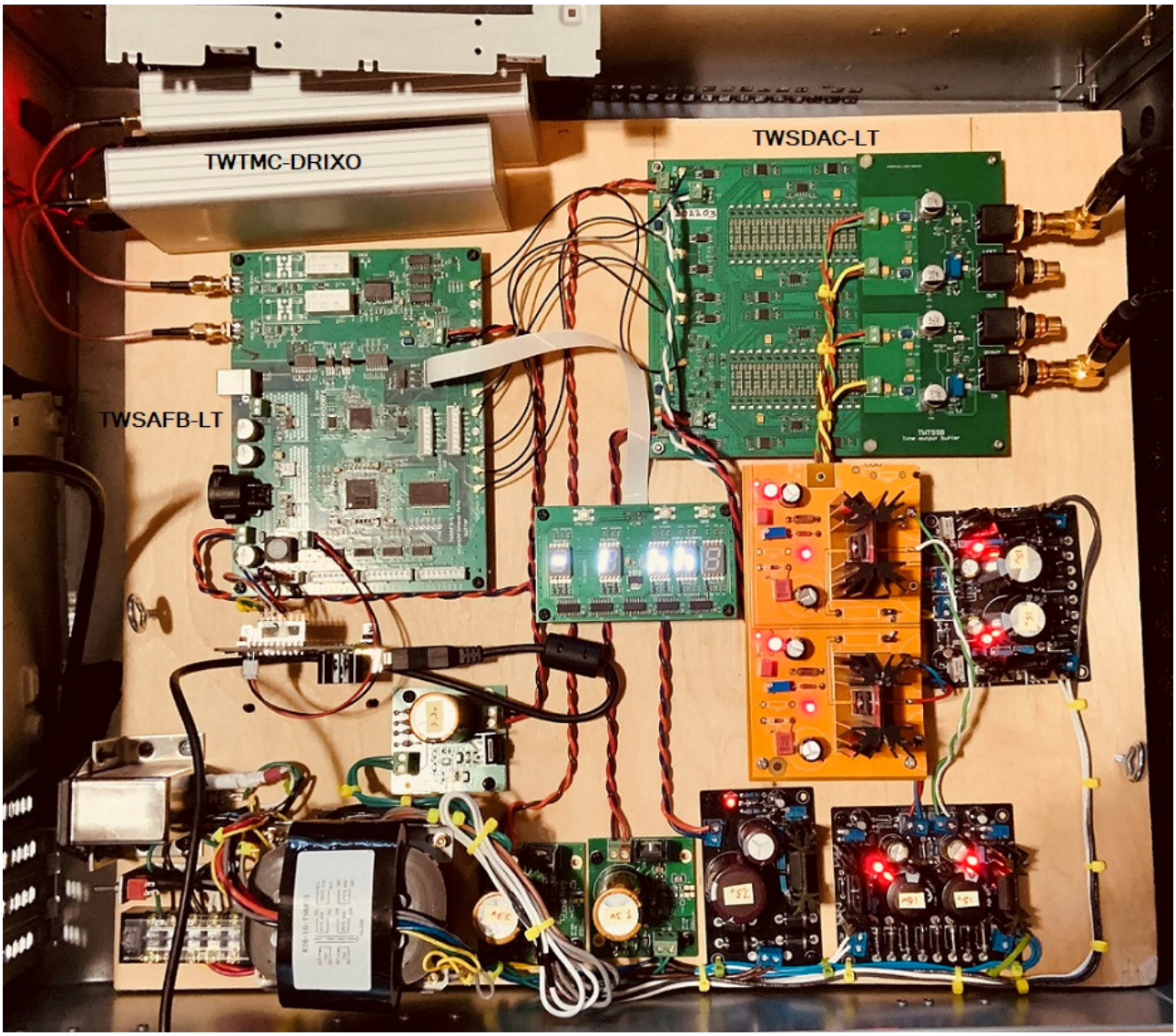
In plugged mode this button is labeled "Save settings in EEPROM" and allows the user to store the current settings in the memory of the FIFO Lite. The same settings check is performed and the user can save the data only when all parameters are formally correct and consistent.

If the settings data are saved correctly the application issues the information message " Data saved successfully". If the save operation fails, the application returns the error message "Failed saving data".

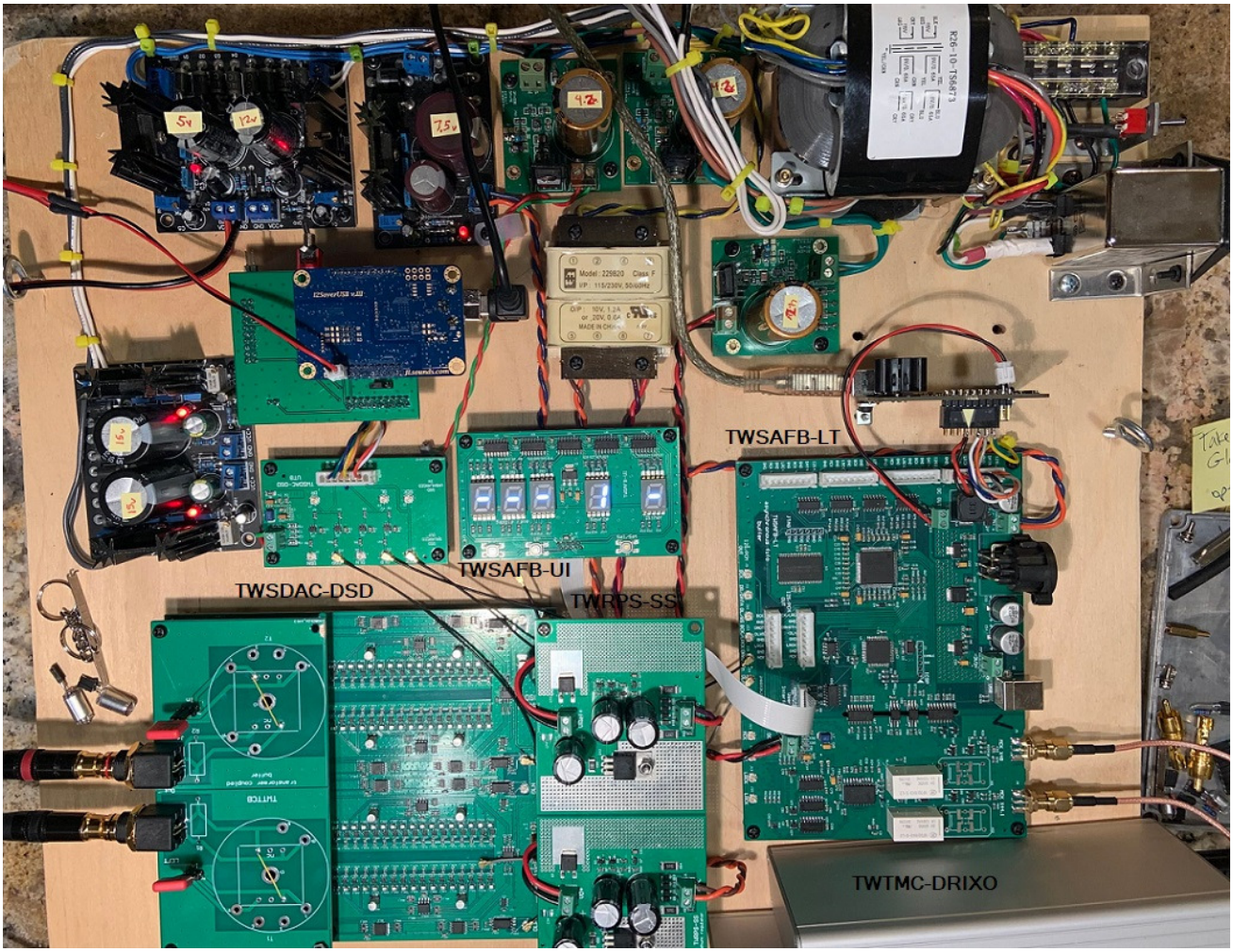
Once the FIFO Lite has been configured you can disconnect the USB cable. You can now connect the FIFO Lite to the source and the planned DAC and enjoy the music.

You can export and print the settings by the dedicated buttons.

You can upload the exported settings later using the appropriate button.



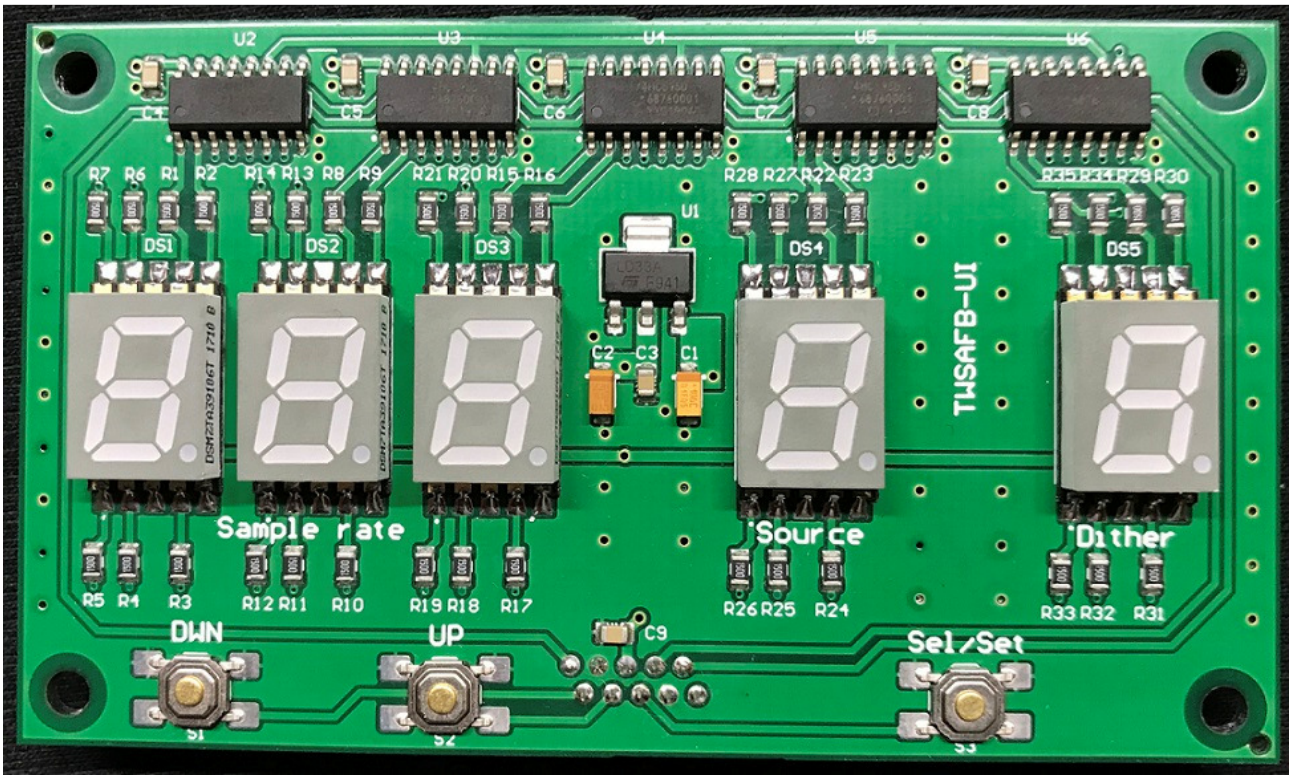
FIFO Lite with a pair of DRIXO oscillators drives the DAC Lite.



FIFO Lite with a pair of DRIXO oscillators drives the DSD discrete DAC.

TWSAFB-UI User Interface (optional)

The TWSAFB-UI User Interface board allows the user to display and change some settings on the fly.

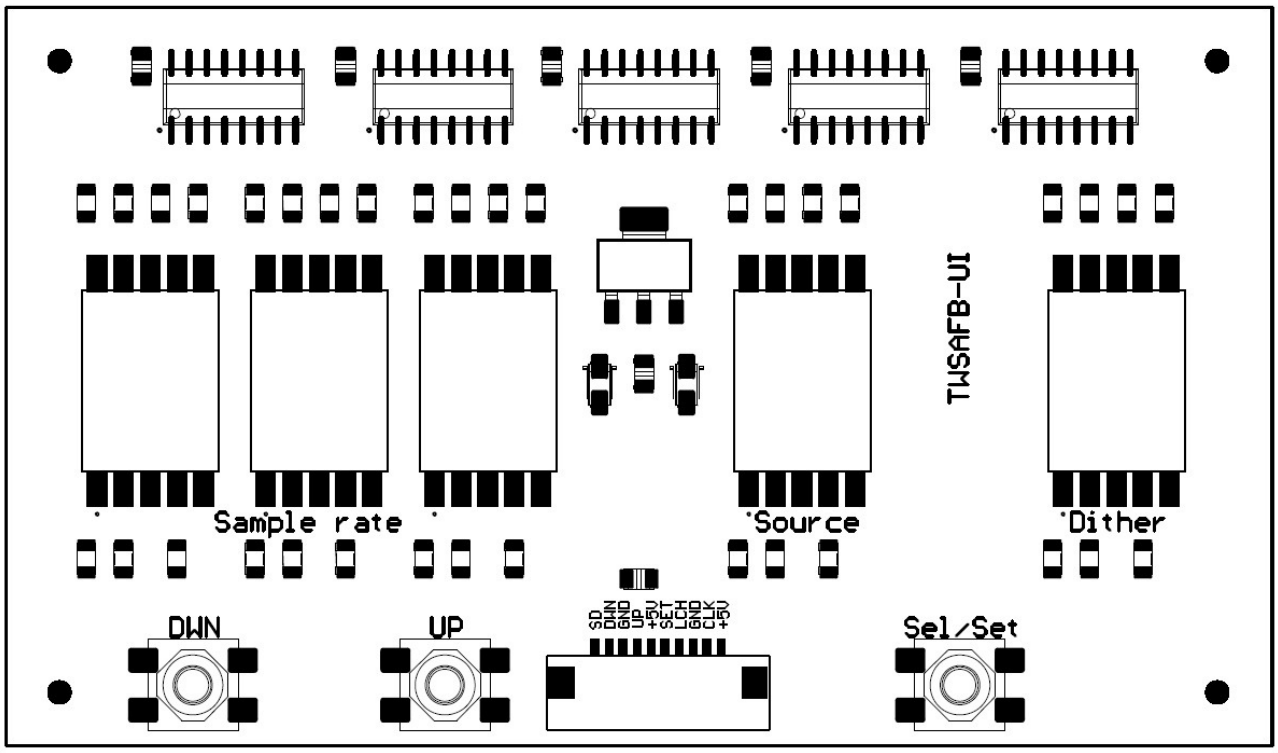


Features:

Inputs and power supply: TWSAFB-LT User Interface flat cable
Display: Sample rate, Selected source, Selected dither option
Settings: source selection, dither, enable/disable DAC calibration, reset
Board size: 91 x 53 mm

Note: finished board

PCB layout



Connectors

J1: 10 way FCC, connect to J1 of the TWSAFB-LT (User Interface)

Display

The first three digits show the current sample rate: 44.1 up to 384 for I2S/PCM input format, 64 to 512 for DSD/DoP input format.
The fourth digit shows the selected source, from 1 to 4.
The fifth digit shows the selected Dither option, from "-" (no dither) to 8.

Buttons

A fast pression of the UP/DWN buttons allows to change the source from 1 to 4. The source is changed for the current session only, default source will be restored as soon as a new startup occurs.

By a fast pression of the Sel/Set button the Dither digit starts blinking, allowing the user to change the Dither option from "-' (no dither to 8). Dither option is changed for the current session only, when a new startup occurs the Dither option is restored to the initial settings configured by the Windows application.

By holding the Sel/Set button for a second or so one can access the menu. Then one can move in the menu pressing the Dwn button. The managed functions managed of the menu are:

- "dEF", which allows to set the default source from 1 to 4
- "rSt", which allows to reset the FIFO board
- "CAL "/"UnCAL", which allows to enable and disable the digital calibration (toggle)
- "ESC", which allows to exit the menu and return back to the standard view

When navigating the menu, for each function, one can press the Up button to change the setting of the active function. For example in the Cal/Uncal function, pressing the Up button one can toggle between Cal and Uncal mode.

Press the Sel/Set button to store the selected option in the FIFO memory. This way the changes are permanent and will be remembered at the next startup.

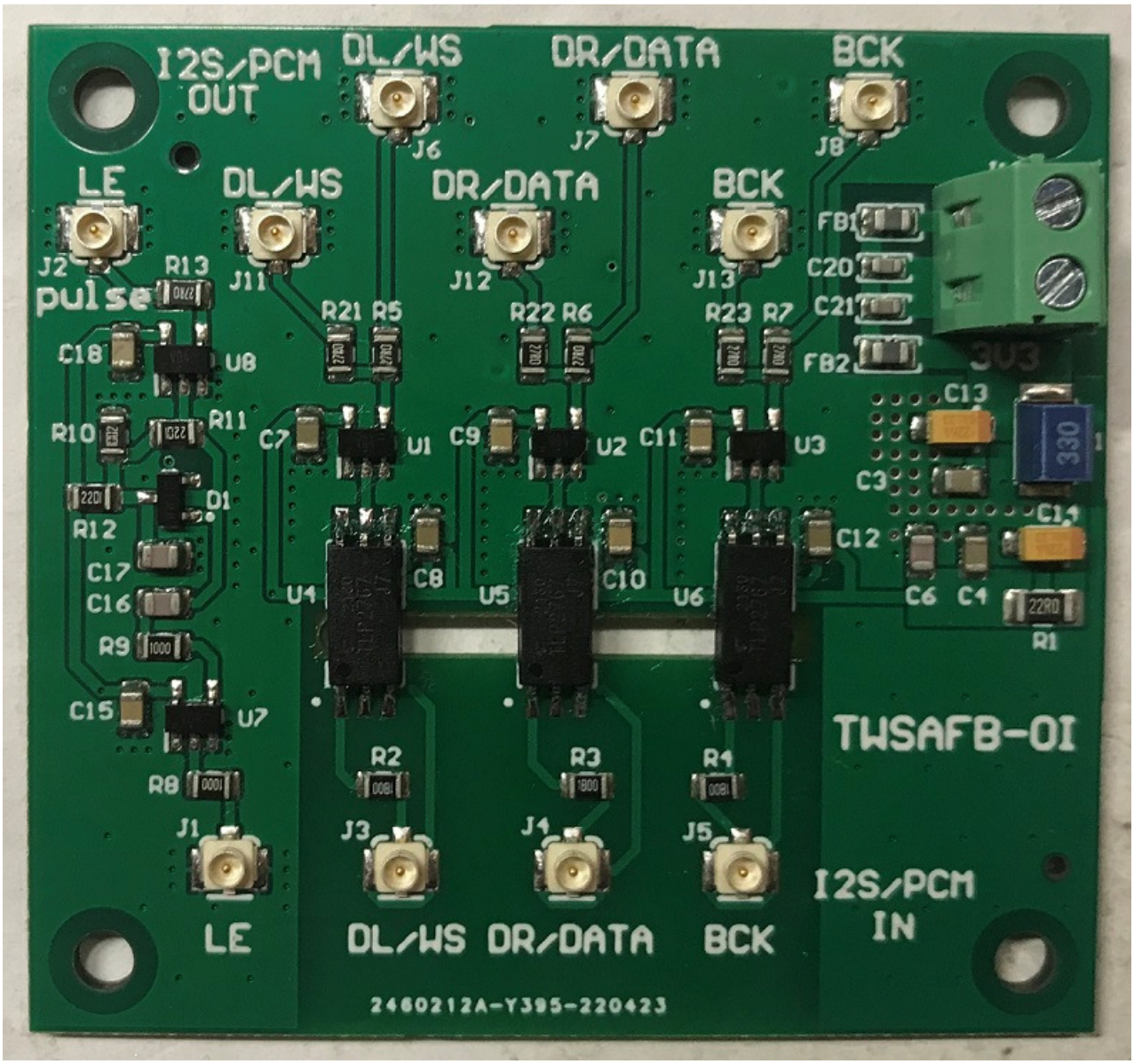
Information and error messages

The User interface also displays the following information and error messages:

- "FIFO LItE", information message, FIFO startup
- "OSCdt", information message, FIFO is detecting the installed oscillators at startup
- "USb", information message, FIFO is connected to the PC by USB cable
- "CFG ", information message, FIFO is configuring the settings at startup
- "donE ", information message, settings have been configured
- "OSCEr", error message, oscillators have not been detected or they they are inconsistent (for example 5.6448 MHz and 12.288 MHz)
- "CFGEr", error message, configuration settings are not valid
- First 3 digits (sample rate) '- - -', error message, sample rate not valid or missing
- "Sr Er", error message, sample rate is above the allowed limit
- "IntEr", error message, SPI communication failure occurs

TWSAFB-OI Optical Isolator (optional)

The TWSAFB-OI is an optional board intended to optically isolate the DAC from the dirty part of the I2S signal coming from the FPGA (BCK, DR, DL).

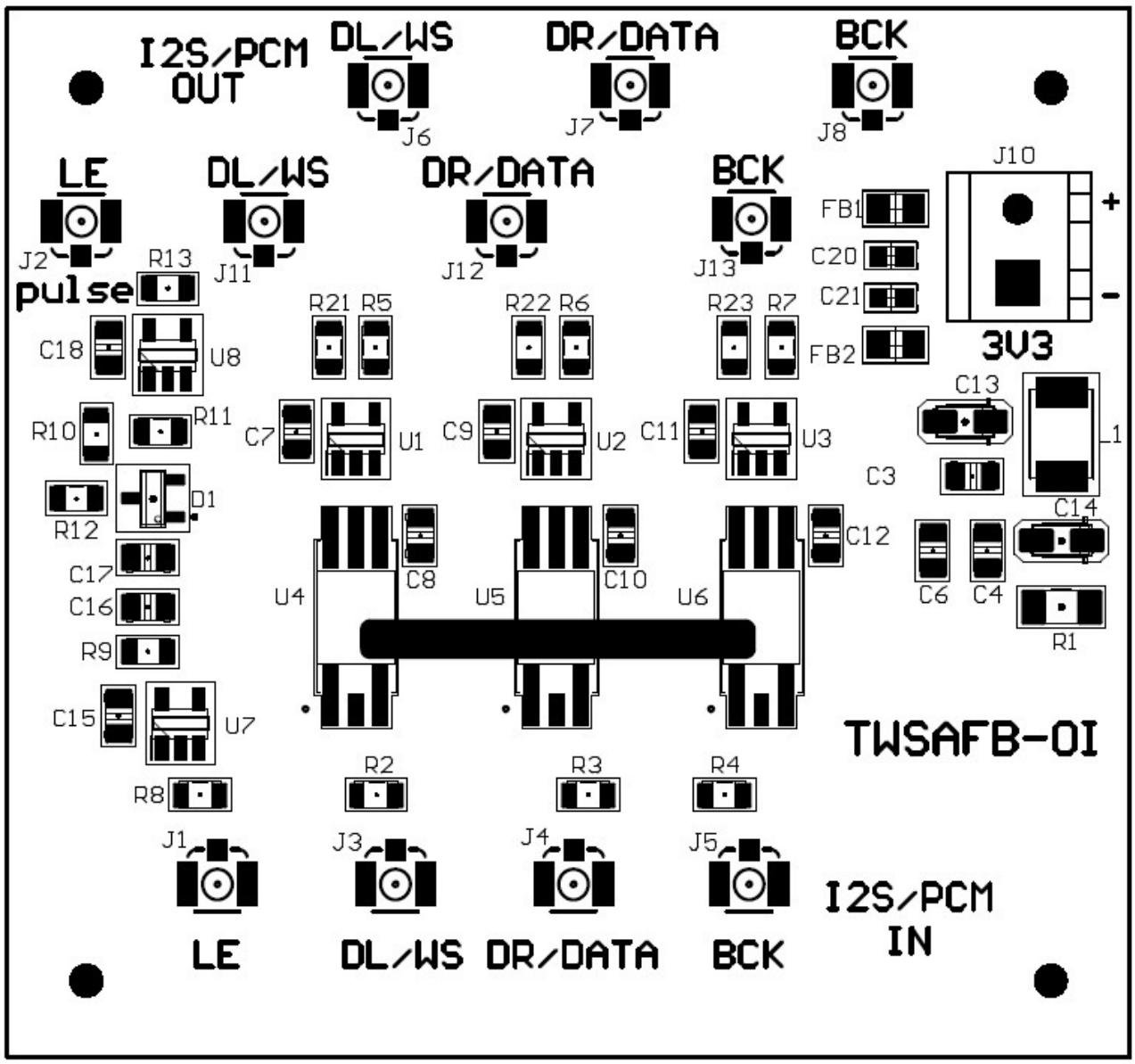


Features:

Inputs: I2S DL/WS, DR/DATA, BCK
Outputs: Optically isolated I2S DL/WS, DR/DATA, BCK
Power supply: clean regulated 3.3VDC/20mA
Board size: 58 x 54 mm

Note: finished board

PCB layout



Recommended for DACs which switch on LRCK or MCK signals like TDA1541A, AD1862, AD1865, ESS Sabre, AKM and so on. It also provides the pulse latch enable signal to drive TDA1541A DAC (not needed with TWSDAC-1862 and TWSDAC-1541, which have isolator and pulse latch enable on board).

Connectors

J1: LE, latch enable input for TDA1541A DAC, connect to J13 or J22 of the FIFO Lite (not needed with TWSDAC-1541)

J2: LE pulse, pulse latch enable output for TDA1541A DAC, connect to LRCK of the TDA1541A DAC board (not needed with TWSDAC-1541)

J3: DL/WS, PCM Left DATA input (stopped clock), I2S WS input (continuous clock), DSD Left DATA input, connect to J10 of the FIFO Lite

J4: DR/DATA, PCM Right DATA input (stopped clock), I2S DATA input (continuous clock), DSD Right DATA input, connect to J11 of the FIFO Lite

J5: BCK, I2S/PCM bit clock input, connect to J9 of the FIFO Lite

J6-J11: isolated DL/WS, PCM Left DATA output (stopped clock), I2S WS output (continuous clock), DSD Left DATA output

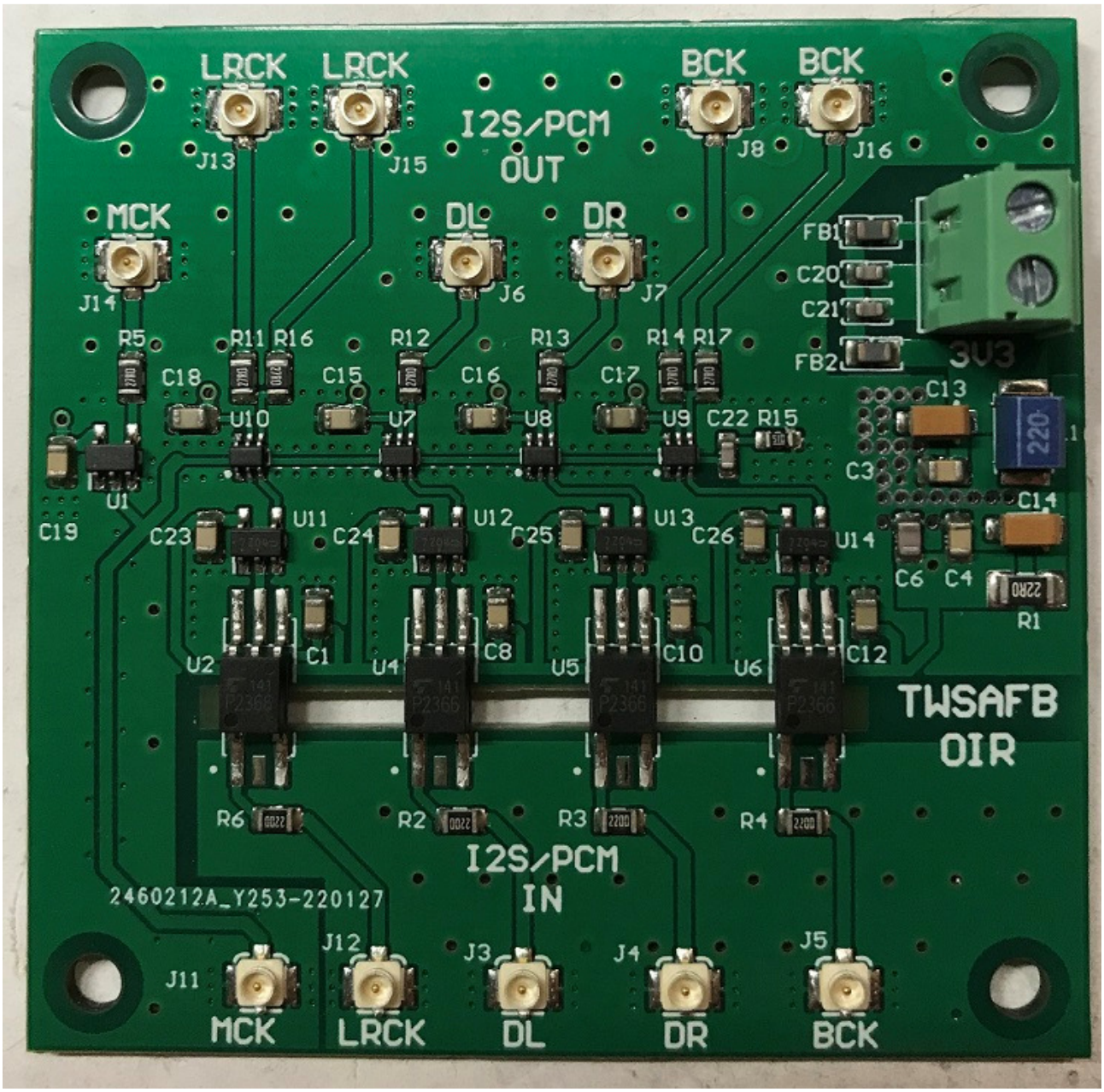
J7-J12: isolated DR/DATA, PCM Right DATA output (stopped clock), I2S DATA output (continuous clock), DSD Right DATA output

J8-J13: isolated BCK, I2S/PCM bit clock output

J10: regulated power supply input, 3.3VDC/20mA

TWSAFB-OIR Optical Isolator & Reclock (optional)

The TWSAFB-OIR is an optional board intended to optically isolate the DAC from the I2S signal coming from the FPGA. All the I2S signals are reclocked by the clean MCK.

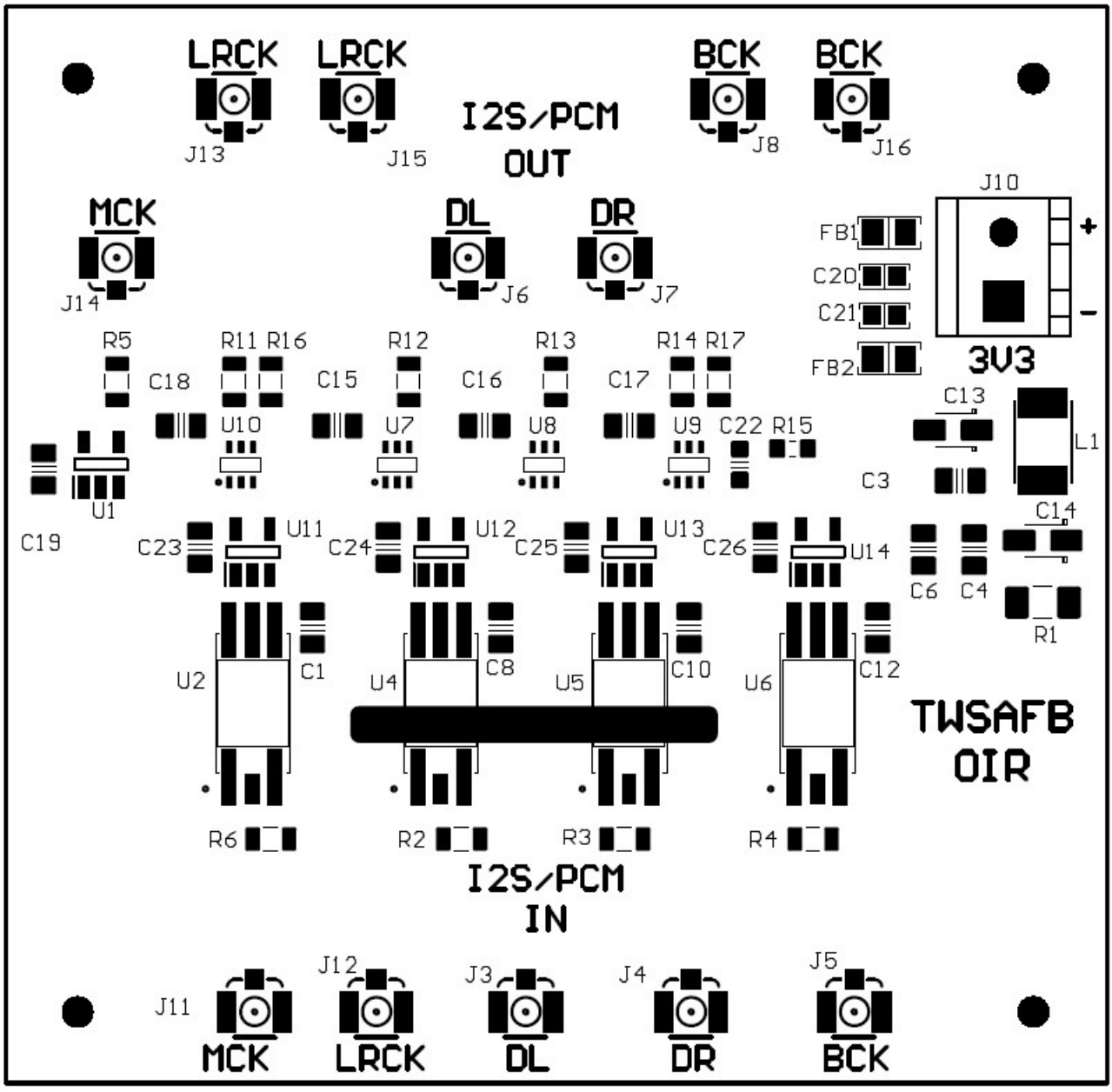


Features:

Inputs: Clean MCK, I2S BCK/LRCK, DL/WS, DR/DATA, BCK
Outputs: Clean MCK, Optically isolated and reclocked I2S BCK/LRCK, DL/WS, DR/DATA, BCK
Power supply: clean regulated 3.3VDC/40mA
Board size: 61 x 60 mm

Note: finished board

PCB layout



Recommended for DACs which switch on BCK signals like PCM1704, PCM1794, PCM63 and so on.

Connectors

J11: MCK, Master clock input, connect to J12 or J21 of the FIFO Lite

J14: MCK, Master clock output

J12: LRCK, LRCK input, connect to J13 or J22 of the FIFO Lite

J3: DL, PCM Left DATA input, connect to J10 of the FIFO Lite

J4: DR, PCM Right DATA input, connect to J11 of the FIFO Lite

J5: BCK, PCM bit clock input, connect to J9 of the FIFO Lite

J13-J15: isolated and reclocked LRCK output

J6: isolated and reclocked PCM Left DATA output

J7: isolated and reclocked PCM Right DATA output

J8-J16: isolated and reclocked BCK PCM bit clock output

J10: regulated power supply input, 3.3VDC/40mA